Amendments to the Specification:

Please replace the Abstract on page 34 with the following Amended Abstract:

ABSTRACT OF DISCLOSURE

A method for interfacing components includes receiving a request for an access operation, and determining whether data corresponding to a requested data address is missing from memory, such as cache. Data may be converted from a first communication type to a second communication type and written to the memory and to a second one of the components during a write operation, and converted from the second communication type to a first communication type and read by the first component during a read operation. The components may be an integrated device ~~electronic~~ electronics (IDE) hard disk drive and a system or controller originally designed to communicate with a modified frequency modulation (MFM) hard disk drive. Handshaking signals such as index and seek-complete signals allow the interface module to emulate operation of an MFM hard disk drive. Method for writing and reading a serial data stream to and from a component associated with a parallel data stream are also described.

Please replace the paragraph on Page 1, starting at line 3 which starts with "This invention relates generally" with the following amended paragraph:

This invention relates generally to the field of interfacing components and, more particularly, to an intelligent module for interfacing an integrated device electronics (IDE) hard disk drive with ~~an~~ a modified frequency modulation (MFM)-based control system.

Please replace the paragraph on Page 6, starting at line 12 which starts with "With respect to inputs received" with the following amended paragraph:

With respect to inputs received from system 20, interface module 30 can accept the following signals: head select 0, head select 1, head select 2; drive select 0, drive select 1; step; direction; ~~MFM~~ write gate, and MFM write data. The three head selects associated with an exemplary embodiment of the present invention are used to form a binary number that can be used to specify one of, for example, eight simulated heads that are to be active on the next read or write operation. Meanwhile, the drive select lines can be used to specify, for example, a drive that system 20 needs to access. Referring now to the step signal, this input can be used to trigger a motor (of an MFM drive) to step read/write heads one track in the direction determined by the state of the direction input.

Please replace the paragraph on Page 12, starting at line 23 which starts with "Although, as can be understood" with the following amended paragraph:

Although, as can be understood by one of ordinary skill in the art, management module 32 can be, for example, implemented in software, or by using discrete logic (e.g., transistor-transistor logic (TTL), ~~complimentary~~ complementary metal-oxide semiconductor (CMOS), etc.) or custom / semi-custom devices (e.g., application-specific integrated circuits or ASICs), and can comprise a single component or a plurality of components, the management module of the illustrated embodiment comprises a single programmable logic device ("PLD"), such as a field programmable gate array ("FPGA"). A PLD from the Flex® 10K family of devices offered by Altera Corporation of San Jose, California, such as the Flex® 10K20, can be used to form management module 32. As can be understood by one of ordinary skill in the art, one advantage of using a Flex® 10K20 PLD can include the

utilization of embedded array blocks (EABs), which can be ideal for RAM, ROM, and first in, first out ("FIFO") functions.

Please replace the paragraph on Page 14, starting at line 26 which starts with "According to an exemplary embodiment" with the following amended paragraph:

According to an exemplary embodiment, a clock frequency of 1.25 MHZ (.8 us period) is used to set a count to 10, with an index-pulse one-shot circuit using a counter to generate an 8us pulse. Meanwhile, a seek-complete one-shot circuit can use a counter clock frequency of 610.35 Hertz (Hz) ~~Hz~~ (1.63 ms period), with the seek-complete pulse being initiated after a count of 2 (3.2ms). As can be understood by one of ordinary skill in the art, these times were chosen to approximate the time delay (used to emulate certain types of MFM hard disks) needed to keep a cache miss from occurring during a head step operation.